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Intel® Xeon® Silver 4210 Processor

13.75M Cache, 2.20 GHz

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Essentials	Export specification
Product Collection	2nd Generation Intel® Xeon® Scalable Processors
Code Name	Products formerly Cascade Lake
Vertical Segment	Server
Processor Number ?	4210
Status	Launched
Launch Date ?	Q2'19
Lithography ?	14 nm
Use Conditions ?	Server/Enterprise
Recommended Customer Price ?	-
# of Cores ?	10
# of Threads 🕐	20
# of Threads ? Processor Base Frequency ?	
	2.20 GHz
Processor Base Frequency ?	2.20 GHz 3.20 GHz
Processor Base Frequency ? Max Turbo Frequency ?	2.20 GHz 3.20 GHz 13.75 MB
Processor Base Frequency ? Max Turbo Frequency ? Cache ?	20 GHz 3.20 GHz 13.75 MB 2
Processor Base Frequency ? Max Turbo Frequency ? Cache ? # of UPI Links ?	2.20 GHz 3.20 GHz 13.75 MB
Processor Base Frequency ? Max Turbo Frequency ? Cache ? # of UPI Links ? TDP ?	2.20 GHz 3.20 GHz 13.75 MB

Max Memory Size (dependent on memory type) (?)	11
Memory Types ?	DDR4-240
Maximum Memory Speed	2400 MF
Max # of Memory Channels 💽	
ECC Memory Supported ‡ ?	Ye
Intel® Optane™ DC Persistent Memory Supported ?	N
Expansion Options	
Scalability	2
PCI Express Revision ?	3
Max # of PCI Express Lanes ?	4
Package Specifications	
Sockets Supported ?	FCLGA364
T _{CASE} ?	78°
Package Size	76.0mm x 56.5ml
Advanced Technologies	
Intel® Deep Learning Boost (Intel® DL Boost) ?	Ye
Intel® Speed Select Technology - Performance Profile 🔞	N
Intel® Speed Select Technology - Base Frequency ?	N
Intel® Resource Director Technology (Intel® RDT)	Ye
Intel® Speed Shift Technology ?	Ye
Intel® Turbo Boost Max Technology 3.0 ‡ ?	N
Intel® Turbo Boost Technology ‡ 🔞	2
Intel vPro® Platform Eligibility ‡ 🔞	Ye
Intel® Hyper-Threading Technology ‡ 👔	Ye
Intel® Virtualization Technology (VT-x) ‡ 🔞	Ye
Intel® Virtualization Technology for Directed I/O (VT-d)‡ ?	Ye
Intel® VT-x with Extended Page Tables (EPT) ‡ 🔞	Ye
Intel® Transactional Synchronization Extensions ?	Ye
Intel® 64 ‡ 🕐	Ye
Instruction Set Extensions	Intel® AVX2, Intel® AVX-51
# of AVX-512 FMA Units 🔞	
Enhanced Intel SpeedStep® Technology ?	Ye
Intel® Volume Management Device (VMD) 💿	Ye



More support options for Intel® Xeon® Silver 4210 Processor (13.75M Cache, 2.20 GHz)





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Refer to Datasheet for formal definitions of product properties and features.

‡ This feature may not be available on all computing systems. Please check with the system vendor to determine if your system delivers this feature, or reference the system specifications (motherboard, processor, chipset, power supply, HDD, graphics controller, memory, BIOS, drivers, virtual machine monitor-VMM, platform software, and/or operating system) for feature compatibility. Functionality, performance, and other benefits of this feature may vary depending on system configuration.

Max Turbo Frequency refers to the maximum single-core processor frequency that can be achieved with Intel® Turbo Boost Technology. See www.intel.com/technology/turboboost/ for more information.

System and Maximum TDP is based on worst case scenarios. Actual TDP may be lower if not all I/Os for chipsets are used.

 $Intel \ processor \ numbers \ are \ not \ a \ measure \ of \ performance. \ Processor \ numbers \ differentiate \ features \ within each \ processor \ family, \ not \ across \ different \ processor \ families. \ See \ http://www.intel.com/content/www/us/en/processors/processor-numbers.html \ for \ details.$

"Announced" SKUs are not yet available. Please refer to the Launch Date for market availability.

Some products can support AES New Instructions with a Processor Configuration update, in particular, i7-2630QM/i7-2635QM, i7-2670QM/i7-2675QM, i5-2430M/i5-2435M, i5-2410M/i5-2415M. Please contact OEM for the BIOS that includes the latest Processor configuration update.

See http://www.intel.com/content/www/us/en/architecture-and-technology/hyper-threading/hyper-threading-technology.html? wapkw=hyper+threading for more information including details on which processors support Intel® HT Technology.

Processors that support 64-bit computing on Intel® architecture require an Intel 64 architecture-enabled BIOS.

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